PCA9535; PCA9535C

16-bit I²C-bus and SMBus, low power I/O port with interrupt

Rev. 6 — 7 November 2017 Product data sheet

1. General description

The PCA9535 and PCA9535C are 24-pin CMOS devices that provide 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I²C-bus I/O expanders. The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PCA9535 and PCA9535C consist of two 8-bit Configuration (Input or Output selection), Input, Output and Polarity Inversion (active HIGH or active LOW operation) registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master. Although pin-to-pin and I²C-bus address compatible with the PCF8575, software changes are required due to the enhancements and are discussed in *Application Note AN469*.

The PCA9535 is identical to the PCA9555 except for the removal of the internal I/O pull-up resistor which greatly reduces power consumption when the I/Os are held LOW.

The PCA9535C is identical to the PCA9535 except that all the I/O pins are high-impedance open-drain outputs.

The PCA9535 and PCA9535C open-drain interrupt output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I²C-bus address and allow up to eight devices to share the same I²C-bus/SMBus. The fixed I²C-bus address of the PCA9535 and PCA9535C are the same as the PCA9555 allowing up to eight of these devices in any combination to share the same I²C-bus/SMBus.

2. Features and benefits

- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Low standby current
- Noise filter on SCL/SDA inputs

- No glitch on power-up
- Internal power-on reset
- 16 I/O pins which default to 16 inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Offered in four different packages: SO24, TSSOP24, HVQFN24 and HWQFN24

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9535D	PCA9535D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA9535PW	PCA9535PW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
PCA9535BS	9535	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1
PCA9535HF	P35H	HWQFN24	plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.75 mm	SOT994-1
PCA9535CD	PCA9535CD	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA9535CPW	PCA9535C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
PCA9535CHF	P35C	HWQFN24	plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.75 mm	SOT994-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9535D	PCA9535D,112	SO24	STANDARD MARKING * IC'S TUBE - DSC BULK PACK	1200	T_{amb} = −40 °C to +85 °C
	PCA9535D,118	SO24	REEL 13" Q1/T1 *STANDARD MARK SMD	1000	T_{amb} = −40 °C to +85 °C
PCA9535PW	PCA9535PW,112	TSSOP24	STANDARD MARKING * IC'S TUBE - DSC BULK PACK	1575	T_{amb} = −40 °C to +85 °C
	PCA9535PW,118	TSSOP24	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	T_{amb} = −40 °C to +85 °C
PCA9535BS	PCA9535BS,118	HVQFN24	REEL 13" Q1/T1 *STANDARD MARK SMD	6000	T_{amb} = −40 °C to +85 °C

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

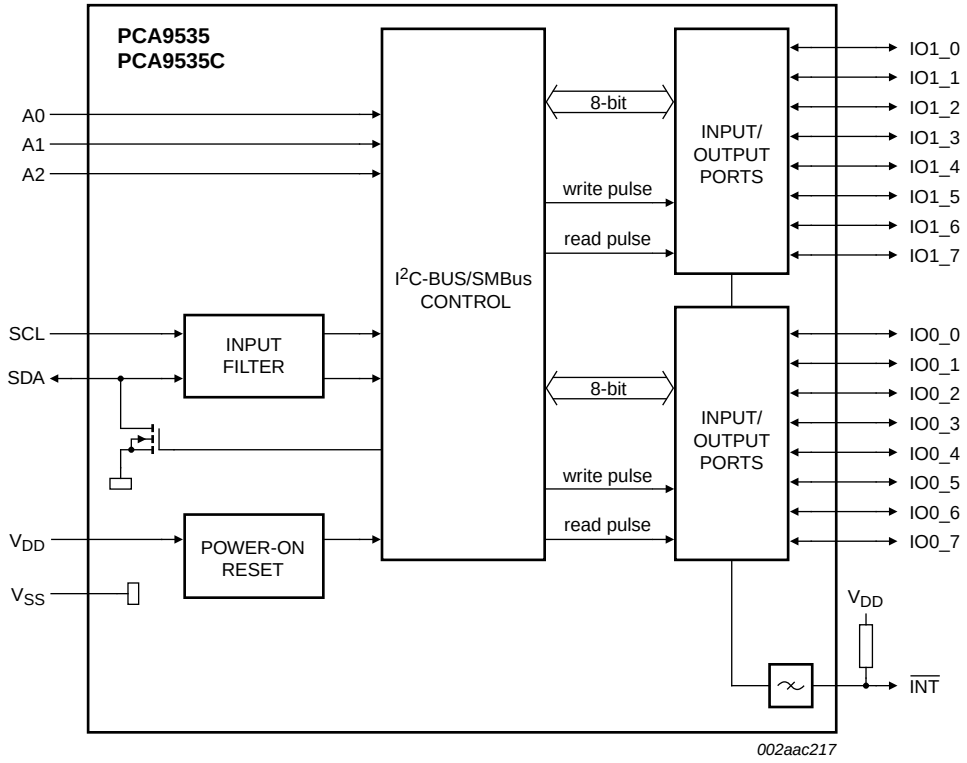
Table 2. Ordering options *…continued*

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9535HF	PCA9535HF,118	HWQFN24	REEL 13" Q1/T1 *STANDARD MARK SMD	6000	T_{amb} = –40 °C to +85 °C
	PCA9535HFHP	HWQFN24	REEL 13" Q2/T3 *STANDARD MARK SMD	6000	T_{amb} = –40 °C to +85 °C
PCA9535CD	PCA9535CD,112	SO24	STANDARD MARKING * IC'S TUBE - DSC BULK PACK	1200	T_{amb} = –40 °C to +85 °C
	PCA9535CD,118	SO24	REEL 13" Q1/T1 *STANDARD MARK SMD	1000	T_{amb} = –40 °C to +85 °C
PCA9535CPW	PCA9535CPW,112	TSSOP24	STANDARD MARKING * IC'S TUBE - DSC BULK PACK	1575	T_{amb} = –40 °C to +85 °C
	PCA9535CPW,118	TSSOP24	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	T_{amb} = –40 °C to +85 °C
PCA9535CHF	PCA9535CHF,118	HWQFN24	REEL 13" Q1/T1 *STANDARD MARK SMD	6000	T_{amb} = –40 °C to +85 °C

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

4. Block diagram



Remark: All I/Os are set to inputs at reset.

Fig 1. Block diagram of PCA9535; PCA9535C

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

5. Pinning information

5.1 Pinning

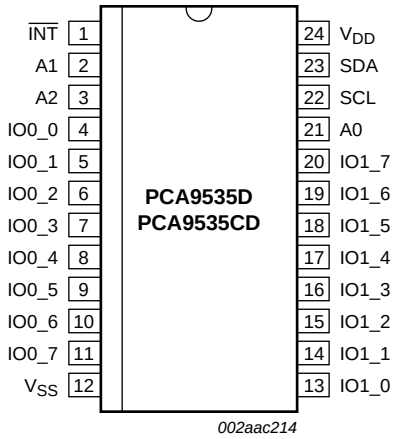


Fig 2. Pin configuration for SO24

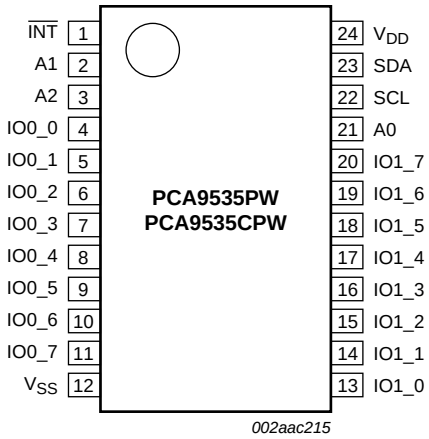


Fig 3. Pin configuration for TSSOP24

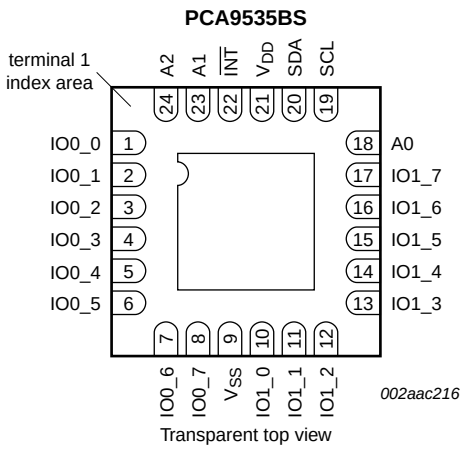


Fig 4. Pin configuration for HVQFN24

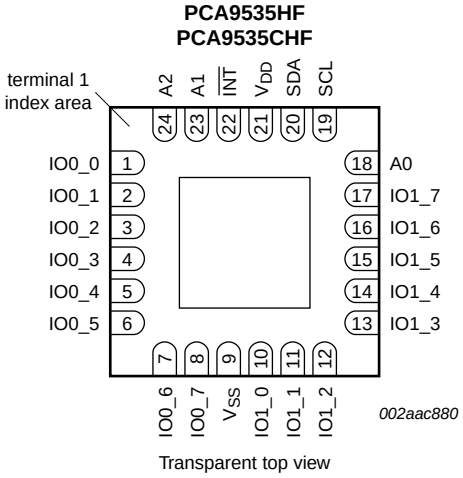


Fig 5. Pin configuration for HWQFN24

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO24, TSSOP24	HVQFN24, HWQFN24	
$\overline{INT}$	1	22	interrupt output (open-drain)
A1	2	23	address input 1
A2	3	24	address input 2
IO0_0	4	1	port 0 input/output[1]
IO0_1	5	2	
IO0_2	6	3	
IO0_3	7	4	
IO0_4	8	5	
IO0_5	9	6	
IO0_6	10	7	
IO0_7	11	8	
V_{SS}	12	9[2]	supply ground
IO1_0	13	10	port 1 input/output[1]
IO1_1	14	11	
IO1_2	15	12	
IO1_3	16	13	
IO1_4	17	14	
IO1_5	18	15	
IO1_6	19	16	
IO1_7	20	17	
A0	21	18	address input 0
SCL	22	19	serial clock line
SDA	23	20	serial data line
V_{DD}	24	21	supply voltage

[1] PCA9535 I/Os are totem pole, whereas the I/Os on PCA9535C are open-drain.

[2] HVQFN24 and HWQFN24 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

6. Functional description

Refer to Figure 1 “Block diagram of PCA9535; PCA9535C”.

6.1 Device address

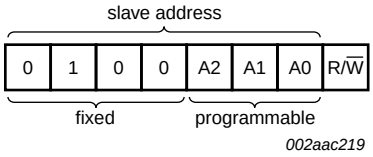


Fig 6. PCA9535; PCA9535C device address

6.2 Registers

6.2.1 Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 4. Command byte

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity Inversion port 0
5	Polarity Inversion port 1
6	Configuration port 0
7	Configuration port 1

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

6.2.2 Registers 0 and 1: Input port registers

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

Table 5. Input port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 6. Input port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

6.2.3 Registers 2 and 3: Output port registers

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 7. Output port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 8. Output port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

6.2.4 Registers 4 and 5: Polarity Inversion registers

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 9. Polarity Inversion port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 10. Polarity Inversion port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

6.2.5 Registers 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. At reset, the device's ports are inputs.

Table 11. Configuration port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 12. Configuration port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

6.3 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9535/PCA9535C in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9535/PCA9535C registers and SMBus state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

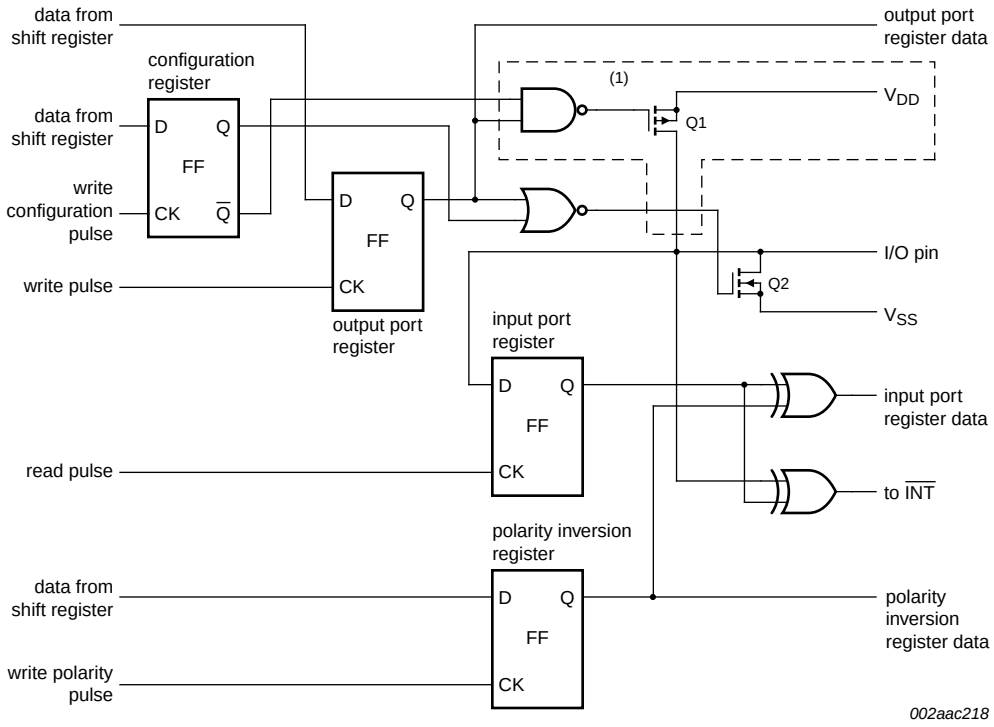
6.4 I/O port

When an I/O is configured as an input on PCA9535, FETs Q1 and Q2 are off, creating a high impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V. In the case of PCA9535C, FET Q1 has been removed and the open-drain FET Q2 will function the same as PCA9535.

If the I/O is configured as an output, then on PCA9535 either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either V_{DD} or V_{SS}.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.



At power-on reset, all registers return to default values.

(1) PCA9535C I/Os are open-drain only. The portion of the PCA9535 schematic marked inside the dotted line box is not in PCA9535C.

Fig 7. Simplified schematic of I/Os

6.5 Bus transactions

6.5.1 Writing to the port registers

Data is transmitted to the PCA9535/PCA9535C by sending the device address and setting the least significant bit to a logic 0 (see Figure 6 “PCA9535; PCA9535C device address”). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the PCA9535/PCA9535C are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see Figure 8 and Figure 9). For example, if the first byte is sent to Output Port 1 (register 3), then the next byte will be stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

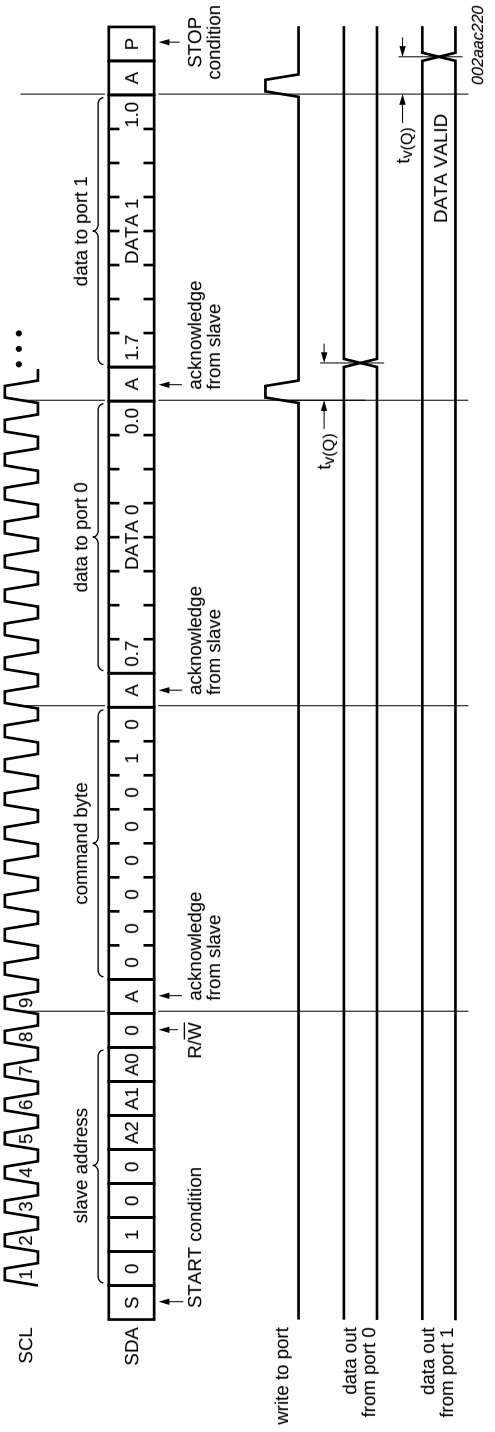


Fig 8. Write to Output Port registers

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

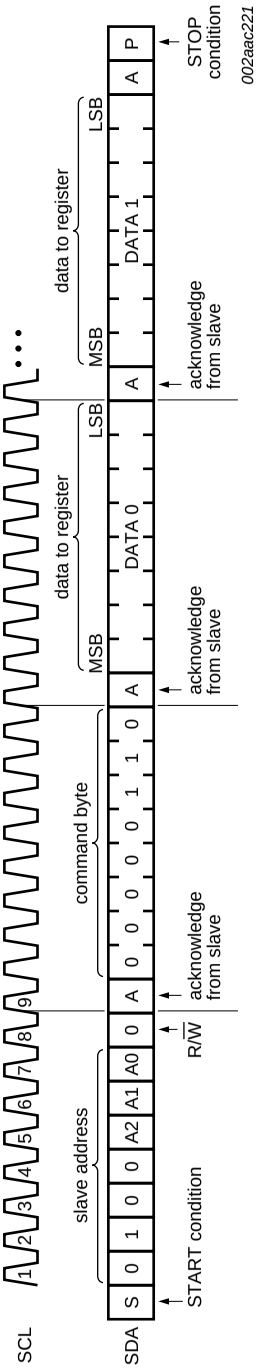


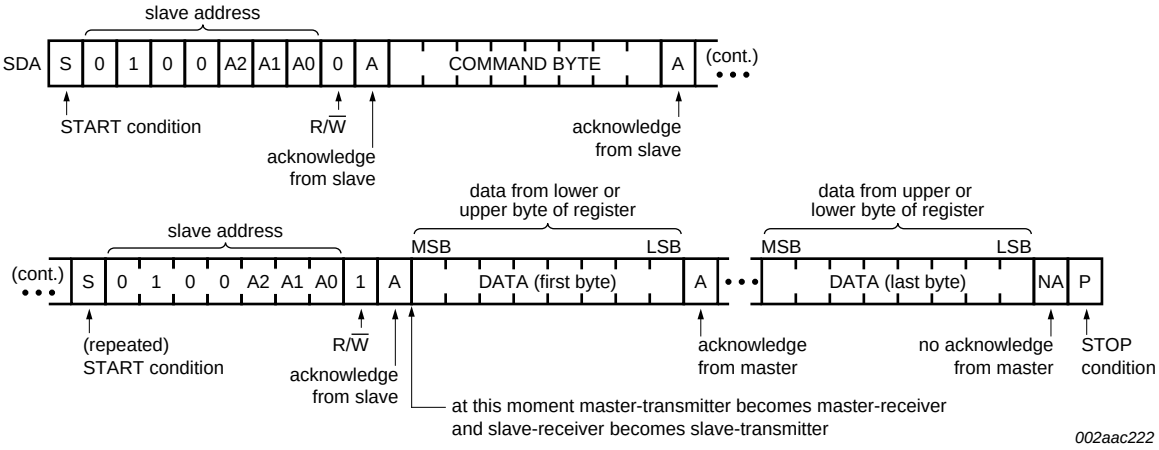
Fig 9. Write to Configuration registers

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

6.5.2 Reading the port registers

In order to read data from the PCA9535/PCA9535C, the bus master must first send the PCA9535/PCA9535C address with the least significant bit set to a logic 0 (see Figure 6 "PCA9535; PCA9535C device address"). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PCA9535/PCA9535C (see Figure 10, Figure 11 and Figure 12). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.

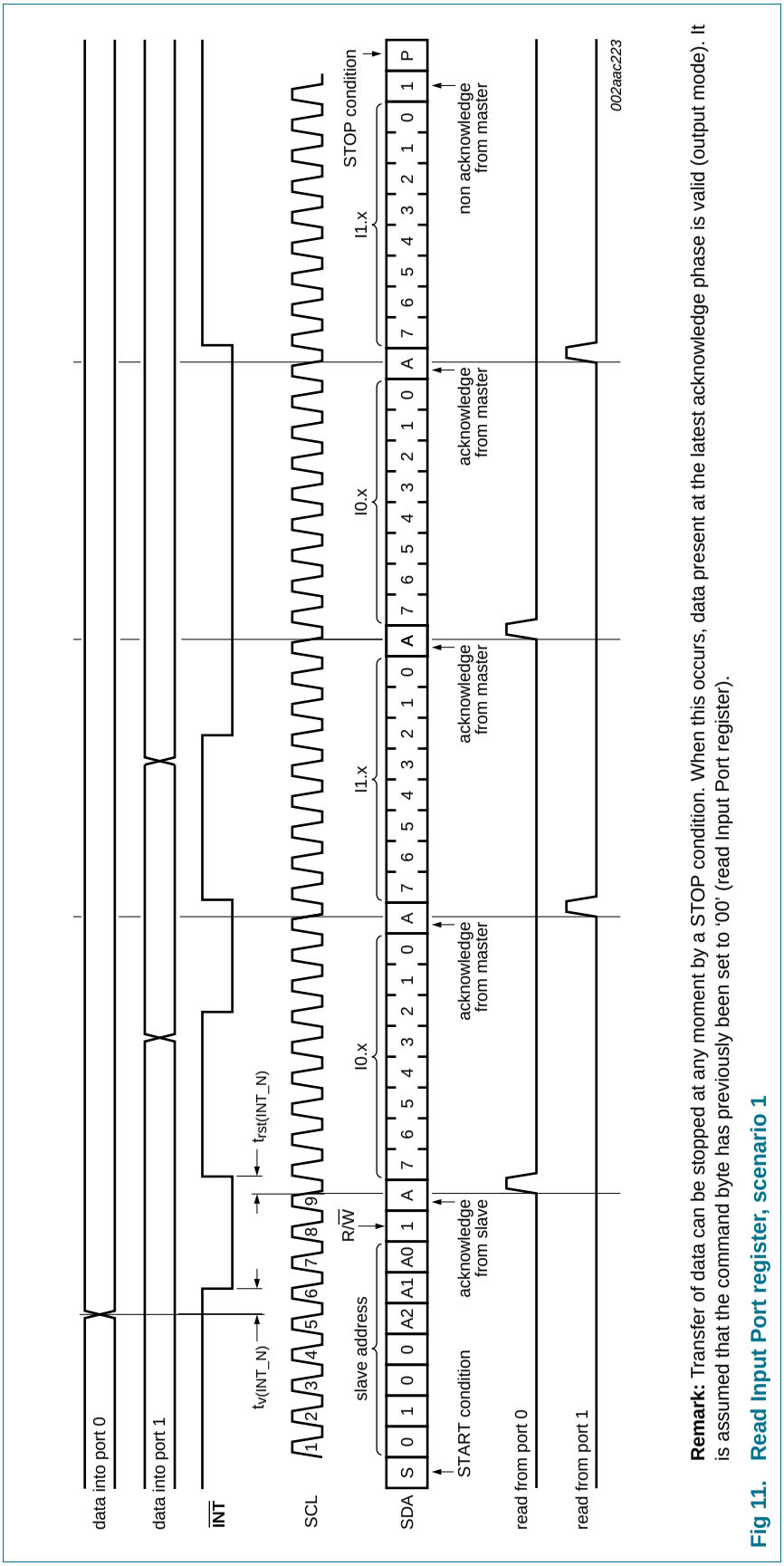


Remark: Transfer can be stopped at any time by a STOP condition.

Fig 10. Read from register

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

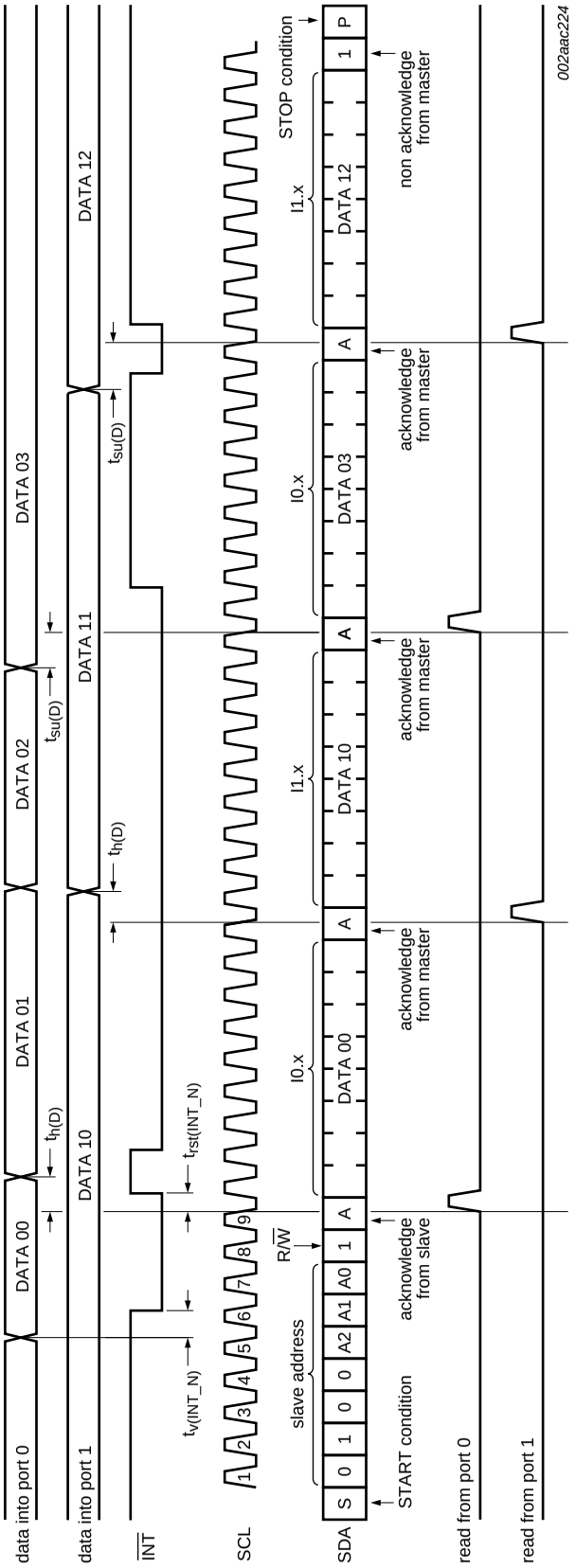


Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Fig 11. Read Input Port register, scenario 1

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Fig 12. Read Input Port register, scenario 2

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

6.5.3 Interrupt output

The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read (see Figure 11). A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Remark: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

7. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 13).

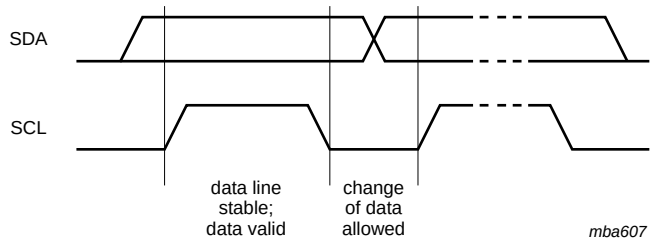


Fig 13. Bit transfer

7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 14).

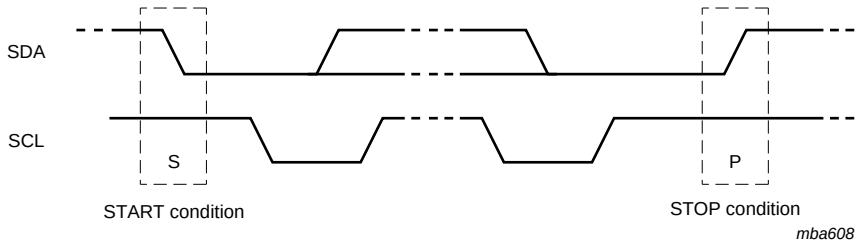


Fig 14. Definition of START and STOP conditions

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

7.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 15).

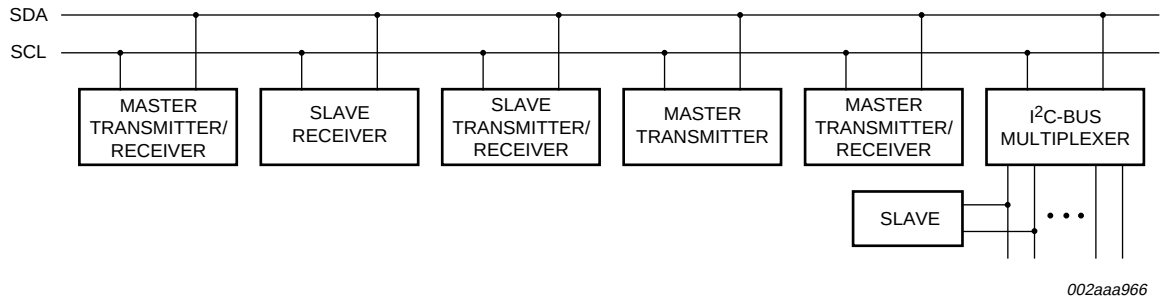


Fig 15. System configuration

7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

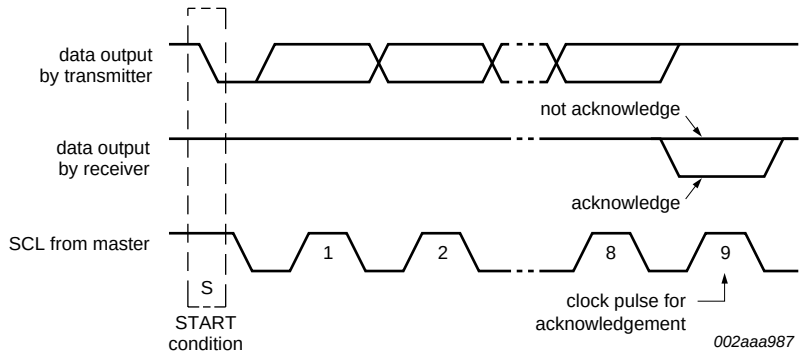
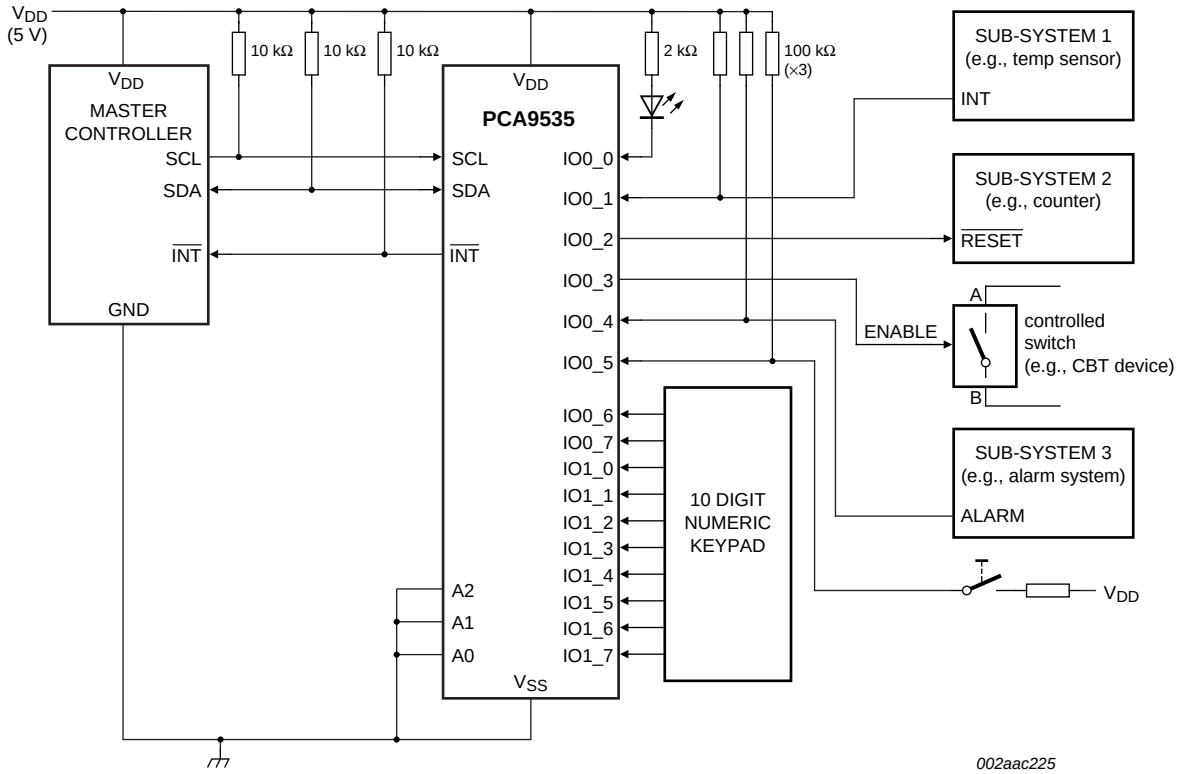


Fig 16. Acknowledgement on the I²C-bus

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

8. Application design-in information



Device address configured as 1110 100Xb for this example.

IO0_0, IO0_2, IO0_3 configured as outputs.

IO0_1, IO0_4, IO0_5 configured as inputs.

IO0_6, IO0_7, and IO1_0 to IO1_7 configured as inputs.

Fig 17. Typical application

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

8.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the PCA9535 I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 17. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 18 shows a high value resistor in parallel with the LED. Figure 19 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.

This concern does not occur in the case of PCA9535C because the I/O pins are open-drain.

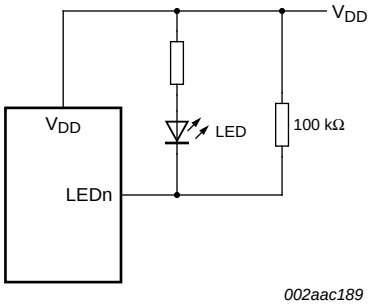


Fig 18. High value resistor in parallel with the LED

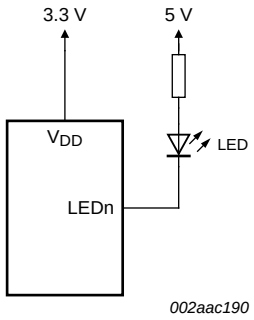


Fig 19. Device supplied by a lower voltage

9. Limiting values

Table 13. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin			V_{SS} − 0.5	6	V
I_O	output current	on an I/O pin		-	±50	mA
I_I	input current			-	±20	mA
I_{DD}	supply current			-	160	mA
I_{SS}	ground supply current			-	200	mA
P_{tot}	total power dissipation			-	200	mW
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature	operating		−40	+85	°C

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

10. Static characteristics

Table 14. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz; I/O = inputs		-	135	200	µA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs		-	0.25	1	µA
		Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$; f_{SCL} = 0 kHz; I/O = inputs		-	0.25	1	µA
V_{POR}	power-on reset voltage[1]	no load; $V_I = V_{DD}$ or V_{SS}		-	1.7	2.2	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
I_L	leakage current	$V_I = V_{DD} = V_{SS}$		−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$		-	6	10	pF
I/Os							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
I_{OL}	LOW-level output current	V_{DD} = 2.3 V to 5.5 V; V_{OL} = 0.5 V	[2]	8	10	-	mA
		V_{DD} = 2.3 V to 5.5 V; V_{OL} = 0.7 V	[2]	10	14	-	mA
V_{OH}	HIGH-level output voltage	PCA9535 only					
		I_{OH} = −8 mA; V_{DD} = 2.3 V	[3]	1.8	-	-	V
		I_{OH} = −10 mA; V_{DD} = 2.3 V	[3]	1.7	-	-	V
		I_{OH} = −8 mA; V_{DD} = 3.0 V	[3]	2.6	-	-	V
		I_{OH} = −10 mA; V_{DD} = 3.0 V	[3]	2.5	-	-	V
		I_{OH} = −8 mA; V_{DD} = 4.75 V	[3]	4.1	-	-	V
		I_{OH} = −10 mA; V_{DD} = 4.75 V	[3]	4.0	-	-	V
I_{LIH}	HIGH-level input leakage current	V_{DD} = 5.5 V; $V_I = V_{DD}$		-	-	1	µA
I_{LIL}	LOW-level input leakage current	V_{DD} = 5.5 V; $V_I = V_{SS}$		-	-	−1	µA
C_i	input capacitance			-	3.7	5	pF
C_o	output capacitance			-	3.7	5	pF
Interrupt $\overline{INT}$							
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
Select inputs A0, A1, A2							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
I_{LI}	input leakage current			−1	-	+1	µA

[1] V_{DD} must be lowered to 0.2 V for at least 5 µs in order to reset part.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

[2] Each I/O must be externally limited to a maximum of 25 mA and each octal (IO0_0 to IO0_7 and IO1_0 to IO1_7) must be limited to a maximum current of 100 mA for a device total of 200 mA.

[3] The total current sourced by all I/Os must be limited to 160 mA. PCA9535C does not source current and does not have the V_{OH} specification.

11. Dynamic characteristics

Table 15. Dynamic characteristics

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	µs
$t_{VD;ACK}$	data valid acknowledge time		[1]	0.3	3.45	0.1	0.9	µs
$t_{HD;DAT}$	data hold time			0	-	0	-	ns
$t_{VD;DAT}$	data valid time		[2]	300	-	50	-	ns
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals			-	300	$20 + 0.1C_b$ [3]	300	ns
t_r	rise time of both SDA and SCL signals			-	1000	$20 + 0.1C_b$ [3]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
Port timing								
$t_{v(Q)}$	data output valid time		[4]	-	200	-	200	ns
$t_{su(D)}$	data input set-up time			150	-	150	-	ns
$t_{h(D)}$	data input hold time			1	-	1	-	µs
Interrupt timing								
$t_{v(INT_N)}$	valid time on pin $\overline{INT}$			-	4	-	4	µs
$t_{rst(INT_N)}$	reset time on pin $\overline{INT}$			-	4	-	4	µs

[1] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.

[4] $t_{v(Q)}$ measured from $0.7V_{DD}$ on SCL to 50 % I/O output (PCA9535). For PCA9535C, use load circuit shown in Figure 24 and measure from $0.7V_{DD}$ on SCL to 30 % I/O output.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

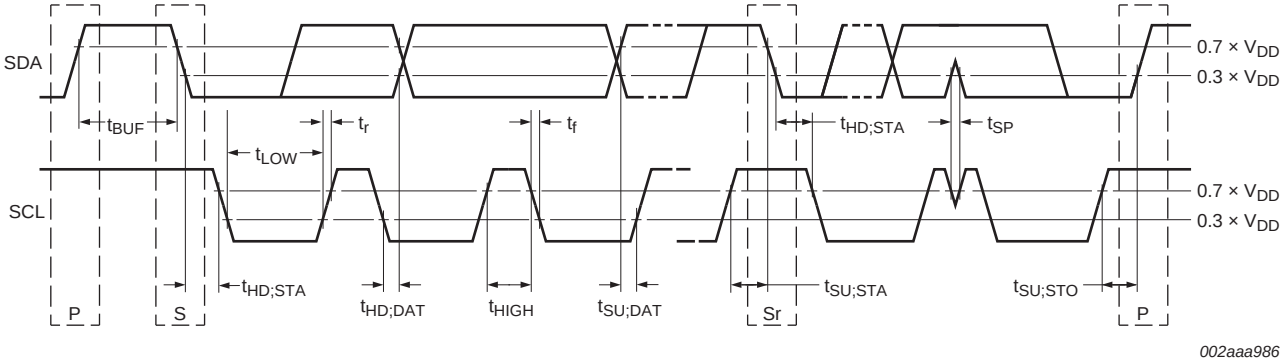
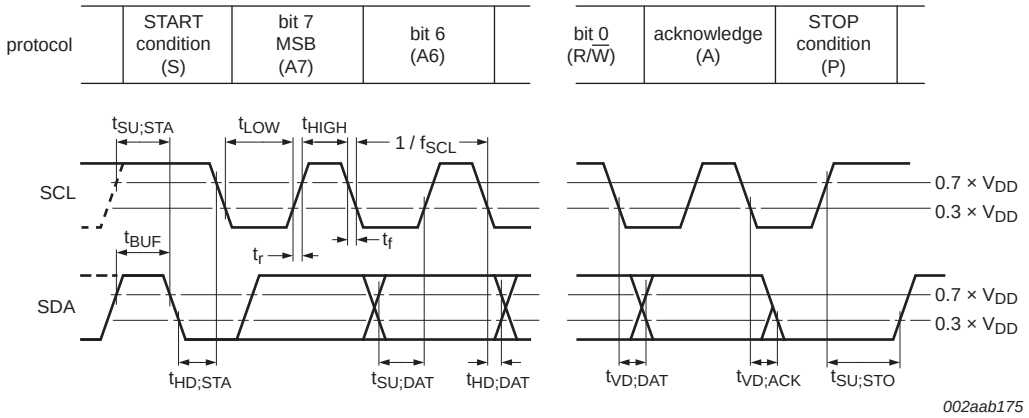


Fig 20. Definition of timing on the I²C-bus



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 21. I²C-bus timing diagram

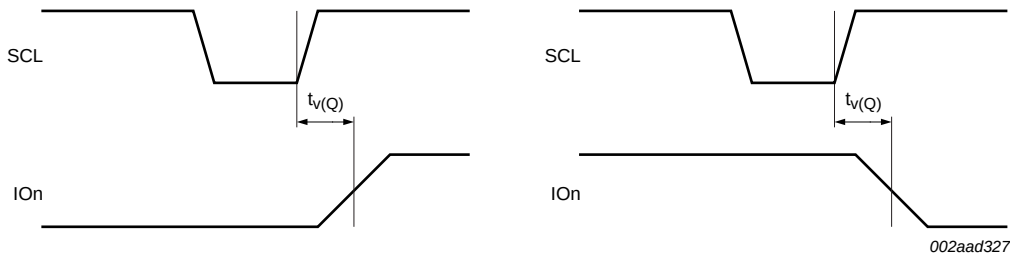
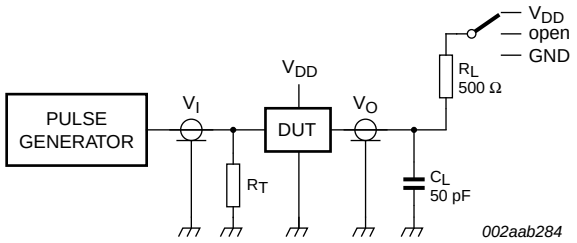


Fig 22. $t_{v(Q)}$ timing

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

12. Test information



R_L = load resistor.

C_L = load capacitance includes jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance of Z_o of the pulse generators.

Fig 23. Test circuitry for switching times

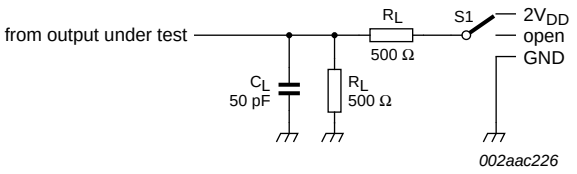


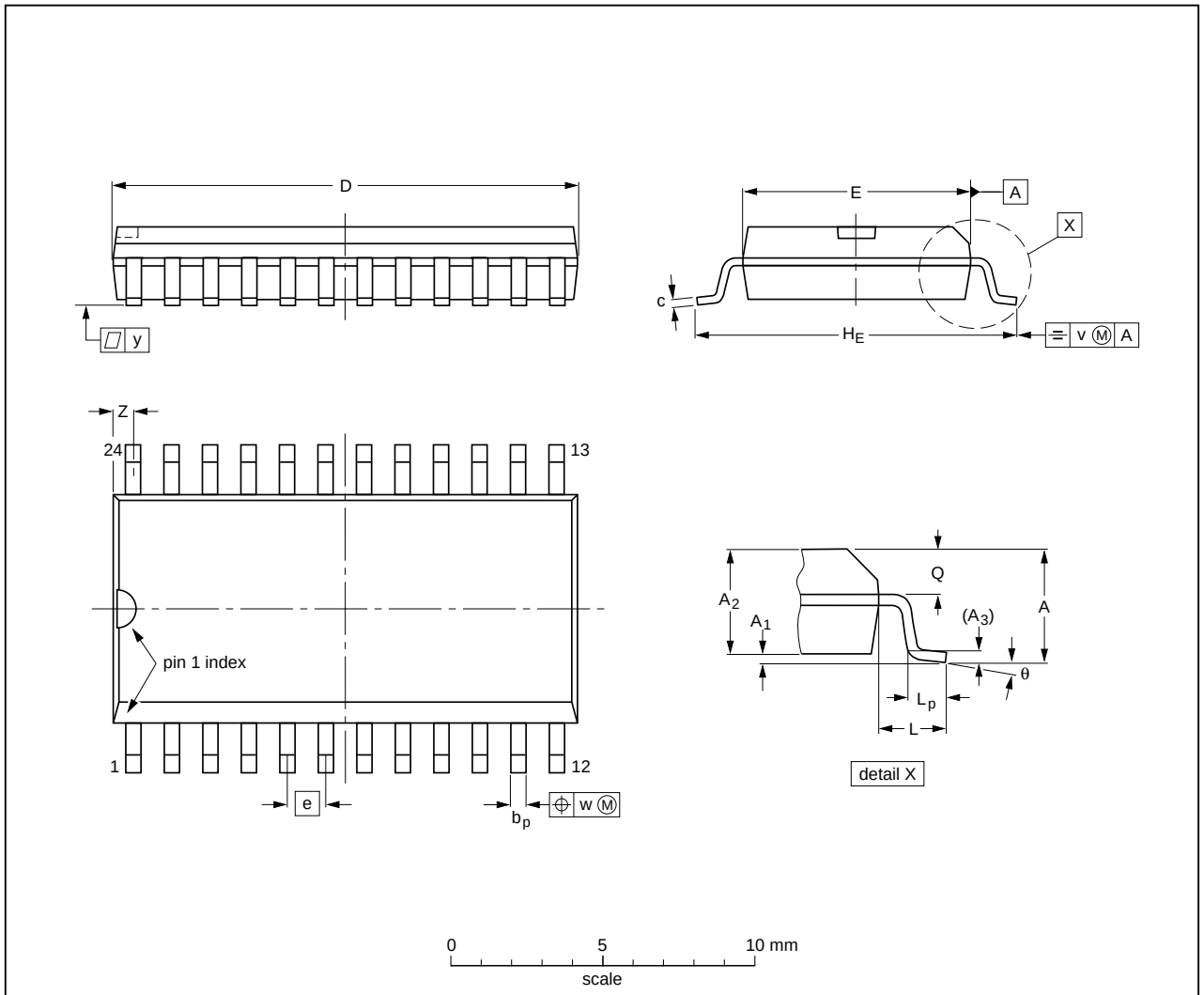
Fig 24. Load circuit

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

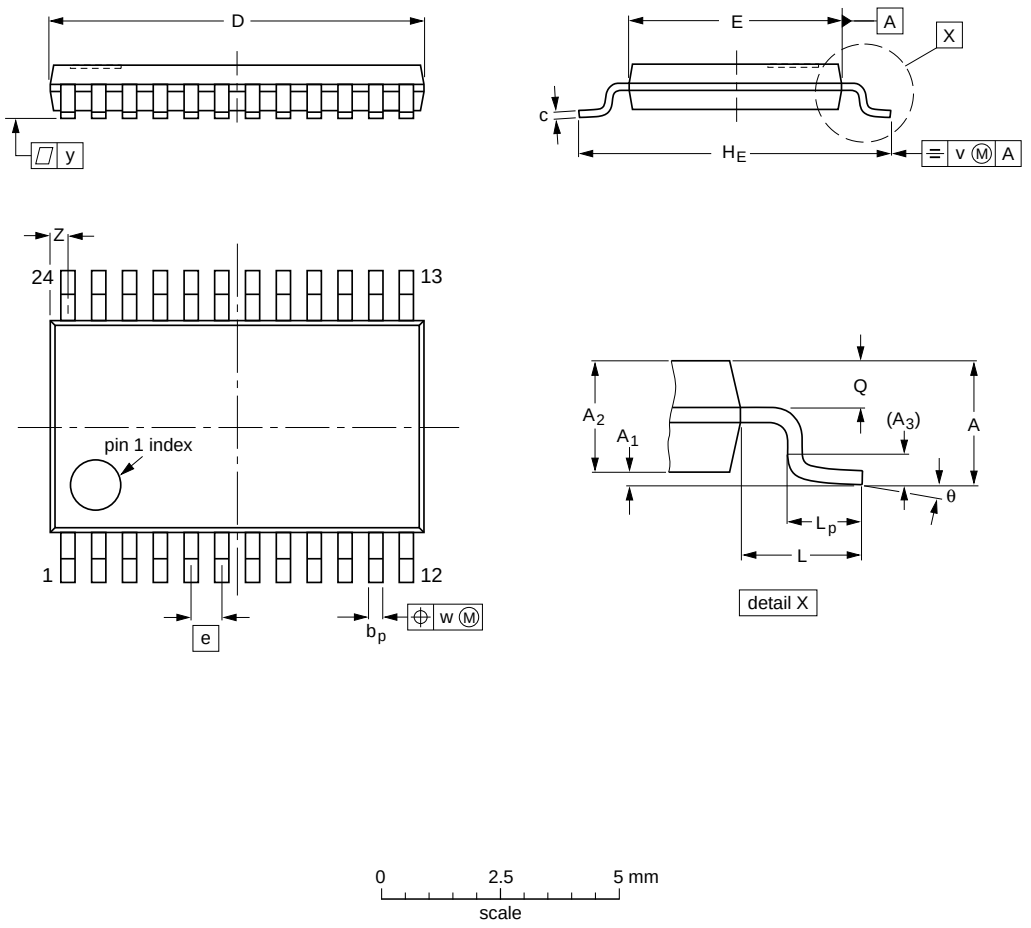
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 25. Package outline SOT137-1 (SO24)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

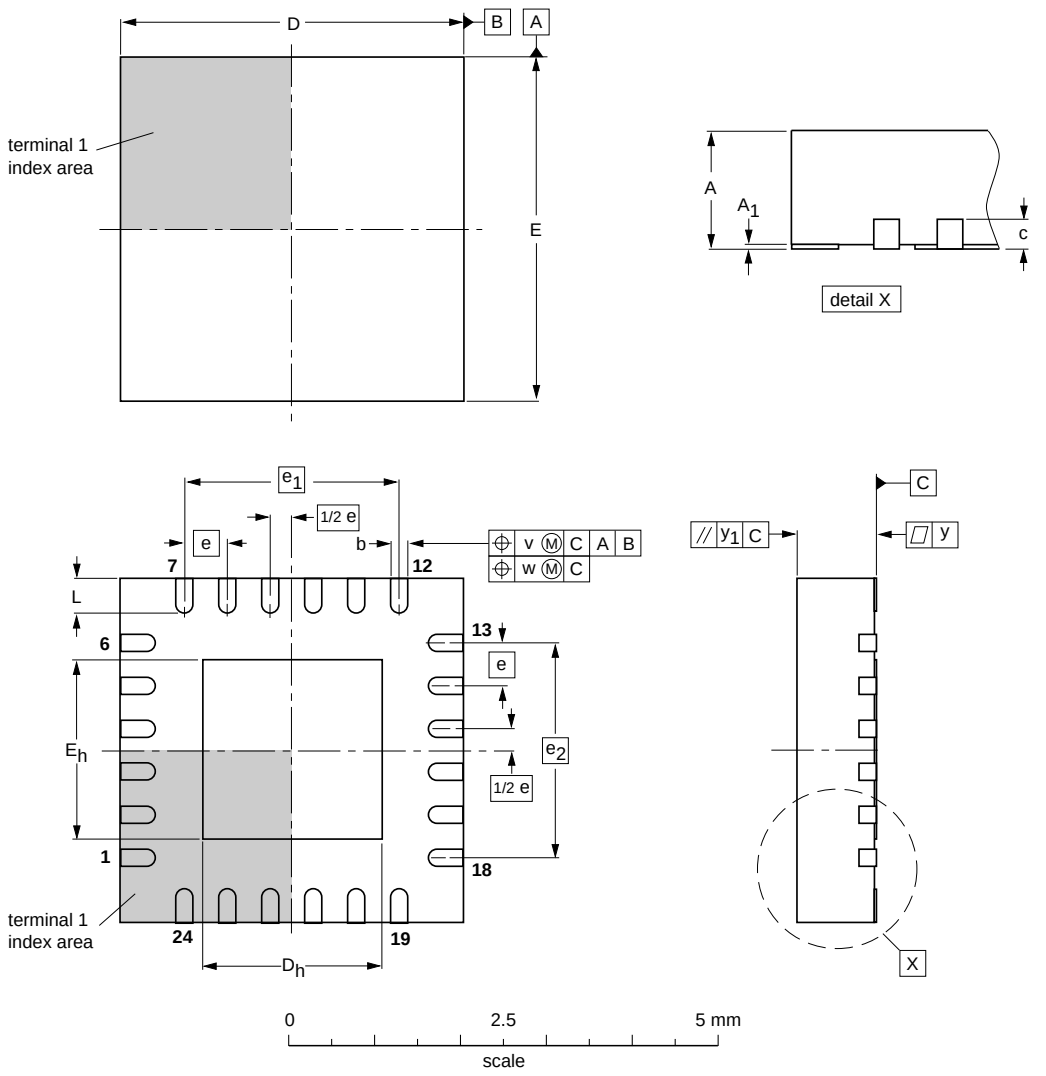
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 26. Package outline SOT355-1 (TSSOP24)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

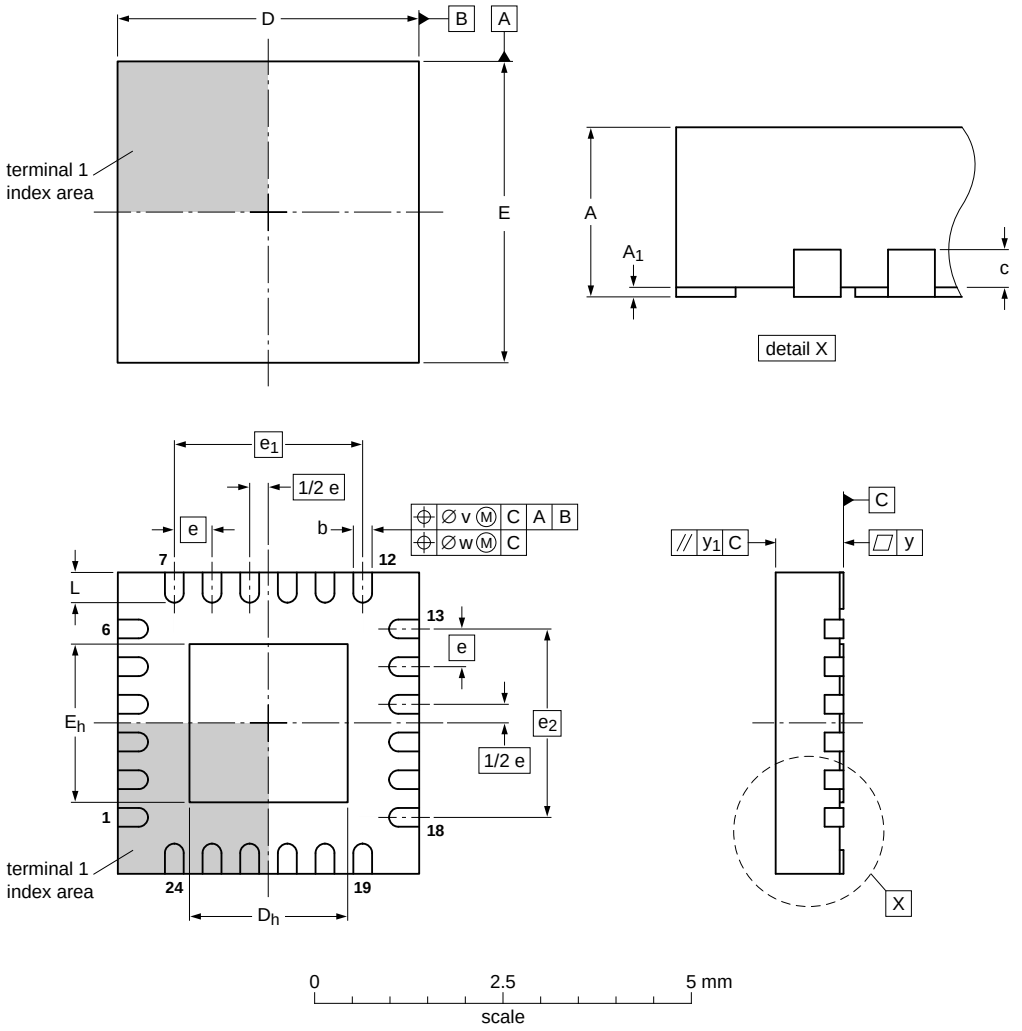
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 27. Package outline SOT616-1 (HVQFN24)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

HWQFN24: plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.75 mm **SOT994-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	0.8	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT994-1	- - -	MO-220	- - -			~~07-02-07~~ 07-03-03

Fig 28. Package outline SOT994-1 (HWQFN24)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

14. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 29) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16 and 17

Table 16. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 17. Lead-free process (from J-STD-020C)

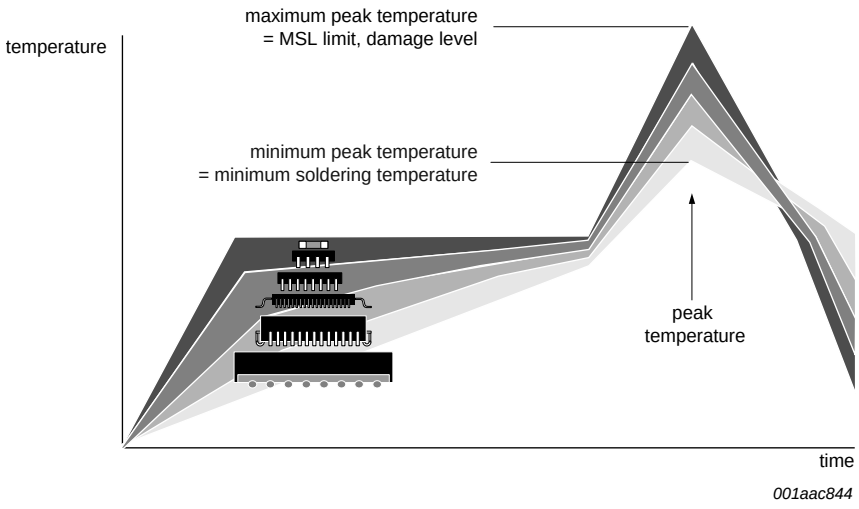
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 29.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.



MSL: Moisture Sensitivity Level

Fig 29. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Abbreviations

Table 18. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CBT	Cross Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
HBM	Human Body Model
I/O	Input/Output
I²C-bus	Inter-Integrated Circuit bus
IC	Integrated Circuit
LED	Light Emitting Diode
MM	Machine Model
PCB	Printed-Circuit Board
SMBus	System Management Bus

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

17. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9535_PCA9535C v.6	20171107	Product data sheet	201710002I	PCA9535_PCA9535C_5
Modifications:	• Table 14 “Static characteristics”: Corrected V_{POR} typ and max limit • Added Section 3.1 “Ordering options”			
PCA9535_PCA9535C_5	20080915	Product data sheet	-	PCA9535_PCA9535C_4
Modifications:	• Table 3 “Pin description”: Table note [1] re-written; added its reference at port 1 input/output			
PCA9535_PCA9535C_4	20080731	Product data sheet	-	PCA9535_PCA9535C_3
PCA9535_PCA9535C_3	20071004	Product data sheet	-	PCA9535_2
PCA9535_2 (9397 750 12896)	20040930	Product data sheet	-	PCA9535_1
PCA9535_1 (9397 750 11681)	20030627	Product data	853-2430 30019 of 11 June 2003	-

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP Semiconductors N.V.

19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2017. All rights reserved.

20. Contents

1 General description 1
2 Features and benefits 1
3 Ordering information 2
3.1 Ordering options 2
4 Block diagram 4
5 Pinning information 5
5.1 Pinning 5
5.2 Pin description 6
6 Functional description 7
6.1 Device address 7
6.2 Registers 7
6.2.1 Command byte 7
6.2.2 Registers 0 and 1: Input port registers 8
6.2.3 Registers 2 and 3: Output port registers 8
6.2.4 Registers 4 and 5: Polarity Inversion registers . 8
6.2.5 Registers 6 and 7: Configuration registers 9
6.3 Power-on reset 9
6.4 I/O port 9
6.5 Bus transactions 10
6.5.1 Writing to the port registers 10
6.5.2 Reading the port registers 13
6.5.3 Interrupt output 16
7 Characteristics of the I²C-bus 16
7.1 Bit transfer 16
7.1.1 START and STOP conditions 16
7.2 System configuration 17
7.3 Acknowledge 17
8 Application design-in information 18
8.1 Minimizing I_{DD} when the I/Os are used to control LEDs 19
9 Limiting values 19
10 Static characteristics 20
11 Dynamic characteristics 21
12 Test information 23
13 Package outline 24
14 Handling information 28
15 Soldering of SMD packages 28
15.1 Introduction to soldering 28
15.2 Wave and reflow soldering 28
15.3 Wave soldering 28
15.4 Reflow soldering 29
16 Abbreviations 30
17 Revision history 31
18 Legal information 32
18.1 Data sheet status 32
18.2 Definitions 32
18.3 Disclaimers 32
18.4 Trademarks 33
19 Contact information 33
20 Contents 34

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2017. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 7 November 2017
Document identifier: PCA9535_PCA9535C